

FORM PTO-1449 (Modified)

LIST OF PATENTS AND PUBLICATIONS FOR
APPLICANT'S INFORMATION
DISCLOSURE STATEMENT

ATTY. DOCKET NO.

RPS920020018US1

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APPLICANT:

GAUR, et al.

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(Use several sheets if necessary) Page 1 of 2

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)
FC	5 7 9 0 8 3 9	Aug. 4, 1998	Luk, et al.			
FC	4 7 5 1 6 8 4	Jun. 14, 1988	Holt			
FC	5 1 6 7 0 2 3	Nov. 24, 1992	de Nicolas, et al.			
FC	5 1 7 2 2 2 8	Dec. 15, 1992	Israelsen			

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation
					YES NO
9 9 1 4 8 8 1	Mar. 23, 1999	PCT			Abstract Only

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

FC	IBM, TDB, Vol. 35, No. 7, Dec. 1992, "Task Switching Between Processes Using the Sequencer"
	IBM TDB, Vol. 35, 1A, June 1992, "Dual-Bus Arbitration for Personal Computer Systems"
FC	Mandl, et al., <u>Elektrotechnik und Informationstechnik</u> , Vol. 115, No. 3, pp. 137-143, 1998, "Real-Time Search-Processor Architectures."

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DATE CONSIDERED

*Frank Gaby**07/09/04*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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<i>PC</i>	Yeong, Kang Lai, et al., <u>Proceedings of 1997 IEEE Intl. Symposium on Circuits and Systems</u> . Circuits and Systems in the Information Age. ISCAS '97, (Cat. No. 97CH35987), Pt. Vol. 2, pp. 1361-1364, Vol. 2, Published: New York, NY, USA, 1997, "An Efficient Array Aarchitecture with Data-Rings for 3-Step Hierarchical Search Block Matching Algorithm."
<i>PC</i>	Kondo, T., et al., <u>IEICE Transactions on Electronics</u> , Vol. E76-C, No. 12, pp. 1827-1834, Dec. 1993, "Single-Board SIMD Processors Using Gate-Array LSIs for Parallel Processing."
<i>PC</i>	Gay, C., <u>Elektronik</u> , Vol. 36, No. 12, pp. 94-96, 98, June 12, 1987, T05, West Germany, "Memory Supervision with the M68000 Processor. II. "Realisation with the PMMU Component."

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